**CURRICULUM VITAE**

Kaushik Chandra Deva Sarma

Assistant Professor

Department of Instrumentation Engineering

Central Institute of Technology, Kokrajhar, BTAD

Assam-783370, India

Phone: 9706490533

Email: kcd.sarma@cit.ac.in

**Educational Qualification**

|  |  |  |  |
| --- | --- | --- | --- |
| Exam Passed | Board/University | Subjects | Division/Class |
| HSLC (10th) | SEBA | GENERAL | I |
| HIGHER SECONDARY (12th) | AHSEC | SCIENCE | I |
| BE | NEHU | ECE | I |
| M.TECH | TEZPUR UNIVERSITY | ELECTRONICS DESIGN AND TECHNOLOGY | I |
| Ph.D. | TEZPUR UNIVERSITY | THESIS TITLE: SCALE LENGTH DETERMINATION, COMPLETE 2-D POTENTIAL MODELLING AND ENHANCEMENT OF SOME PERFORMANCE PARAMETERS OF JUNCTIONLESS TRANSISTORS | THESIS  SUBMITTED |

Work Experience

|  |  |  |  |
| --- | --- | --- | --- |
| Position held | Duration | | University/ Institution |
| From | To |
| Assistant Professor | 24/01/2011 | Till Date | CIT, Kokrajhar |

**Research Areas**: Semiconductor Devices, Optoelectronics

Teaching:

1. Power Electronics

2. Fiber Optics & Laser Instruments

3. Microprocessor & Microcontrollers

4. Electronic Components & Materials

5. Microwave Engineering

6. Electromagnetic Waves

7. Basic Electronics

**List of Selected Publications**

**Journal Publications**

[1] K C D Sarma and S. Sharma, "An Analytical Approach for Drain Current Modelling of A Symmetric Double Gate Junctionless Transistor", Journal of Nanoelectronics and Optoelectronics, American Scientific Publishers (Accepted)

[2] K C D Sarma and S. Sharma, "Carrier Mobility Enhancement of Symmetric Double Gate Junctionless Transistor”, Journal of Nanoelectronics and Optoelectronics, American Scientific Publishers (Accepted)

[3] K C D Sarma and S. Sharma, "An Approach for Complete 2-D Analytical Potential Modelling of Fully Depleted Symmetric Double Gate Junction Less Transistor", Journal of Computational Electronics, Springer, Vol. 14, No. 3, pages 717-725, 2015, September

[4] K C D Sarma and S. Sharma, "Scale Length Determination of Gate All Around (Regular Hexagonal Cross Section) Junctionless Transistor", International Journal of Applied Engineering Research (IJAER) , Vol. 10, No. 2, pages 4751-4762, 2015, February

[5] K C D Sarma, A Mallik, A Bhatnagar "Microcontroller Based Optical power meter for Lab Applications", Journal of Instrument Society of India, Vol. 40, June,2010.

**Conference Publications**

[1] K C D Sarma and S. Sharma, "Scale Length Determination of Gate All Around (Regular Pentagonal Cross Section) Fully Depleted Junctionless Transistor", In IEEE International Conference on Advances in Engineering and Technology Research (ICAETR), Dr. Virendra Swarup Group of Institutions, Unnao, UP, pages 1-5, 1-2 August,2014

[2] K C D Sarma and S. Sharma, "Scale Length Determination of Gate All Around (Octagonal Cross Section) Junctionless Transistor", In International Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV), NIT, Meghalaya, pages 1-5, 29-30th January ,2015

[3] K C D Sarma and S. Sharma,"A Method for Determination of Depletion Width of Single and Double Gate Junction Less Transistor", In International Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV), NIT, Meghalaya, pages 114-119, 29-30th January ,2015

[4] K C D Sarma, S. SharmaandC.Hazarika, "Scale Length Determination of a Fully Depleted Surrounding Gate (Rectangular Cross Section) Junction Less Transistor", In International Conference on Electrical, Electronics, Signals, Communication & Optimization-EESCO, pages 1-4, 24-25 Jan-2015,Visakhapatnam,  Andhra Pradesh, India